REMARKS/ARGUMENTS

Claims 9-24 are currently pending. Claims 9-24 stand rejected. By this amendment, claims 9, 16, 20, 23 and 24 are amended.

The Abstract of the Disclosure is objected to because it was not presented on a separate sheet. A separate sheet containing the Abstract of the Disclosure is attached hereto as part of the Appendix following page 10 of this paper.

Claims 20-24 are objected to because of informalities. Claim 20 is amended to change "to another using [a single-ended input] at least one level shifter circuit having a single ended input, including a first native NMOS transistor device having a threshold less than OV, a second transistor device coupled to the first transistor device and a level shifter circuit coupled to at least the first and second transistor devices comprising: determining if the input signal is greater than a threshold valve of [a] said native NMOS transistor device" to read "to another level using at least one level shifter circuit having a single ended input, said level shifter circuit including a first native NMOS transistor device having a threshold less than OV, a second transistor device coupled to the first native transistor device and a level shifter circuit coupled to at least the first native and second transistor devices comprising: determining if the input signal is greater than a threshold valve of said second NMOS transistor device." Claim 23 is amended to change "VOD" to "VDD," while claim 24 is amended to change "the native NMOS transistor device" to "said second NMOS transistor device" as suggested by the Examiner. Claims 21-22 and 24 depend from claim 20, directly or indirectly, and recite additional features. Applicants respectfully submit that the objections to claims 20-24 have been overcome.

Claims 9-24 are currently pending. Claims 9-24 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-8 of U.S. Patent No. 6,650,167. Applicants do not agree with the Examiner's rejection, but nevertheless are submitting a Terminal Disclaimer in compliance with 37 C.F.R. 1.321(c), disclaiming the terminal part of this application that extends beyond the expiration date of commonly owned U.S.

Patent No. 6,650,167, to obviate the double patenting rejection. Applicants respectfully submit that the obvious type-double patenting rejection is overcome.

Claims 20-24 stand rejected under 35 U.S.C. §112, second paragraph as being indefinite. Claim 20 is amended to change "[a] said native NMOS transistor device" to read "said second NMOS transistor device" as suggested by the Examiner. Claims 21-24 depend from claim 20, directly or indirectly, and recite additional features thereto. Claims 21-22 and 24 depend from claim 20, directly or indirectly, and recite additional features. Applicants respectfully submit that the §112 rejection of claims 20-24 has been overcome.

Claims 9-24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hirano (U.S. Patent No. 5,650,742) ("*Hirano*") in view of Cress et al. (U.S. Patent No. 6,483,386) ("*Cress*"). Applicants traverse this rejection and respectfully submit that the pending claims are allowable.

The Office Action provides that *Hirano* teaches "a level shifter circuit (101), which meets a method of translating a voltage level of a single ended input signal (I1) using at least one pass NMOS transistor device (Qn101)..."[1] Applicants respectfully disagree. *Hirano* does not disclose a single ended input signal as provided in the Office Action. Rather, *Hirano* teaches two input signals, "I1 and S1 indicate input signals..."[2] Even if it is assumed, *arguendo*, that *Hirano* only teaches one input signal as suggested in the Office Action, it does not teach "a single ended input circuit" as recited by amended claims 9 and 16 among other features, nor "using at least one level shifter circuit having a single ended input" as recited by amended claim 20 among other features.

The Office Action further discloses that *Cress* teaches "a pass transistor device (M3) is a native NMOS transistor device having a threshold voltage less than 0V"[3] The Office Action provides that the combination of *Hirano* and *Cress* was obvious to "fully pass the input signal through the pass transistor device

[1] Office Action, pg. 4, lines 24-25 and pg. 5, line 1.
[2] *Hirano*, col. 6, line 49 and Figs. 1 and 8.
[3] Office Action, page 5, lines 10-12.

since native NMOS pass transistor provides a signal with low distortion."[4] Applicants disagree and submit that the suggested combination is not obvious. The Federal Circuit has, on a number of occasions, addressed the issue of whether an alleged case of *prima facie* obviousness was properly made. The Federal Circuit has stated that "[o]bviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination."[5]

Therefore, the fact that the prior art may be combined as suggested in the Office Action, does not make such combination obvious unless it is taught or suggested by the prior art. It is respectfully submitted that the Office Action does not provide any motivation to combine *Hirano* and *Cress*. Generally, the "motivation to combine or modify" references includes identifying some missing element or function that calls out for such combination or modification. Otherwise is difficult to set forth a convincing rationale for a person of ordinary skill to be motivated to make the combination or modification, and it would appear that the claims merely are being used as a template.

The Office Action does not identify any missing element, function or suggestion in *Hirano* related to fully passing the input signal using an NMOS device. The prior art cannot teach a solution to a problem that would not exist based on the prior art disclosure. Specifically, if *Hirano* doesn't teach of suggest a problem related to fully passing the input signal, then the Office Action cannot attribute a solution thereto using a native NMOS transistor device as taught by *Cress*. Therefore, one of ordinary skill in the art would not have any basis for attempting the combination of references taught by the Examiner.

In view of the foregoing, it is respectfully submitted that the pending claims define allowable subject matter. Applicants respectfully request that the present case pass to allowance. Should anything remain in order to place the present

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[4] Office Action, page 5, lines 18-20.
[5] *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 221 USPQ 929, 933 (Fed. Cir. 1984)

application in condition for allowance, the Examiner is kindly invited to contact the undersigned at the telephone number listed below.

Please charge any required fees not paid herewith or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Dated: May 6, 2005

Respectfully submitted,

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